UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/648,401 | 08/27/2003 | Seok-Woo Lee | 053785-5148 | 5327 |

9629 7590 06/20/2005

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

| EXAMINER | |
|---|---|
| ISAAC, STANETTA D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/648,401 | LEE, SEOK-WOO | |
| | Examiner | Art Unit | |
| | Stanetta D. Isaac | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26* is/are allowed.

6)☒ Claim(s) *1-7,9-22,24 and 25* is/are rejected.

7)☒ Claim(s) *8 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the RCE filed on 5/23/05. Currently, claims 1-26 are pending.

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/23/05 has been entered.

### *Specification*

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9-18, 20-22, 24 and 25, rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al., US Patent 5,817,549.

Yamazaki discloses the semiconductor method as claimed. See figures 1A-7, and corresponding text, where Yamazaki teaches, pertaining to claims 1 and 11, a method of forming a polysilicon thin film transistor, comprising: depositing an amorphous silicon layer **23** over a substrate **21** (figure 3A; col. 12, lines 25-27)-; crystallizing the amorphous silicon layer into a polycrystalline silicon layer (figure 3A; col. 12, lines 27-42); patterning the polycrystalline silicon layer to form a polysilicon active layer **24/25** for a thin film transistor (figure 3B; col. 12, lines 43-48); depositing silicon oxide over the polysilicon active layer to form a gate insulation layer **26** under a vacuum condition (figure 3B; col. 12, lines 49-56); applying heat to anneal the gate insulation layer under the vacuum condition, wherein the applying heat to anneal the gate insulation layer is conducted under an atmosphere including at least $H_2$ (figure 2B; col. 12, lines 57-67; col. 13, lines 1-24) and forming a gate electrode **27/28** on the annealed gate insulating layer (figure 3C; col. 13, lines 25-30) ; applying dopants to the polysilicon active layer to form source **30** and drain regions **30** (figures 3D-3E; col. 31-54); forming an interlayer insulator **33** to cover the gate electrode, the gate insulation layer and the source and drain regions (figure 3F; col. 13, lines 55-63; forming source and drain contact holes **34/35/36** in the interlayer insulator to expose portions of the source region and drain region, respectively; and forming source and drain electrodes (figure 3F; col. 55-63).

Yamazaki teaches, pertaining to claims 2 and 12, wherein there is no vacuum break between depositing silicon oxide to form gate insulation layer and applying heat to anneal the gate insulation layer (figures 1A-1B; col. 4, lines 10-20; col. 5, lines 1-12, *Note*: since there are

two chambers that are connected by a passageway where the gas flows from the first chamber to the second chamber there is no break in vacuum).

Yamazaki teaches, pertaining to claims 3 and 13, wherein applying the heat to anneal the gate insulation layer is performed at a temperature ranging from 400 to 600 degrees Celsius (col. 12, lines 62-67; col. 13, lines 1-7). ~~Yamazaki teaches, pertaining to claims 4 and 14, wherein the vacuum condition for applying the heat to annealing the gate insulation layer is a pressure ranging from 50 to 5000mTorr (col. 13, lines 5-8).~~

Pertaining to claims 4 and 14, Yamazaki teaches the method, wherein the vacuum condition for applying the heat to annealing the gate insulation layer is a pressure ranging from 50 to 5000 mTorr (col. 13, lines 5-8).

Pertaining to claims 5 and 15, Yamazaki teaches the method, wherein depositing the silicon oxide includes using a plasma enhanced chemical vapor deposition (PECVD) method. (col. 12, lines 49-56).

Pertaining to claims 6 and 16, Yamazaki teaches the method, wherein crystallizing the amorphous silicon layer includes applying heat to the amorphous silicon layer using an excimer laser (col. 12, lines 33-42).

Pertaining to claims 7 and 22, Yamazaki teaches the method, wherein applying heat occurs in the atmosphere of a vacuum chamber that also including at one of $N_2$, $O_2$, $N_2O$, and NO. (col. 13, lines 1-3, $N_2O$ gas)

Pertaining to claims 9 and 24, Yamazaki teaches the method, wherein the temperature of annealing the gate insulation layer is higher than the temperature of depositing the silicon oxide (col. 12, line 49-56; col. 13, lines 1-7).

Pertaining to claims 10 and 25, Yamazaki teaches the method, wherein there is vacuum break between depositing the silicon oxide to form the gate insulation layer and applying the heat to anneal the gate insulation layer (col. 12, lines 55-56; col. 13, lines 5-11; ***Note***: since the pressure of was increased from 4 Pa to 1 atm pressures, there is a vacuum break between the steps.).

Pertaining to claim 17, Yamazaki teaches the method, wherein the buffer layer includes at least one of silicon oxide ($SiO_x$) and silicon nitride ($SiN_x$) (col.. 12, lines 22-24).

Pertaining to claim 18, Yamazaki teaches the method, wherein applying dopants includes applying p-type ions (figures 3D-3E; col. 13, lines 30-49).

Pertaining to claims 20 and 21, Yamazaki teaches the method, wherein applying dopants includes applying n-type ions that are phosphorous ions. (col. 13, lines 35-42)

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 5,817,549 in view of Stanley Wolf, Silicon Processing For The VLSI Era, 1986, Lattice Press, Vol. II, pg, 436.

Yamazaki discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-7, 9-18, 20-22, 24 and 25, under 35 U.S.C. 102(b).

However, Yamazaki fails to show, pertaining to claim 19, Yamazaki teaches the method, wherein applying dopants includes applying p-type ions that are boron ions.

Wolf teaches, a conventional method of the formation of source/drain regions for CMOS device where boron is conventionally known as a p-type impurity.

It would have been obvious to one of ordinary skill in the art to substitute applying dopants includes applying p-type ions that are boron ions, in the method of Yamazaki, according to the conventional teachings of Wolf, with the motivation of creating a source/drain junction for a CMOS device, for the purpose of forming an electrical connection within the device. In addition, since both arsenic, taught by Yamazaki, and boron are both p-type impurities, boron would prove to be equivalent.

### *Allowable Subject Matter*

Claims 8 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Applicant's dependent claims 8 and 23, and independent claim 26, indicate allowable subject matter over the prior art of record, since, the prior art fails to teach or render obvious the method "wherein, the difference of flat band voltage (Δ Vfb) between initial flat band voltage [Vfb(initial)] and flat band voltage after Fowler-Nordheim stress [Vfb(FNS)] is less than 0.5V after applying the heat to anneal the gate insulation layer."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Stanetta Isaac
Patent Examiner
June 7 2005